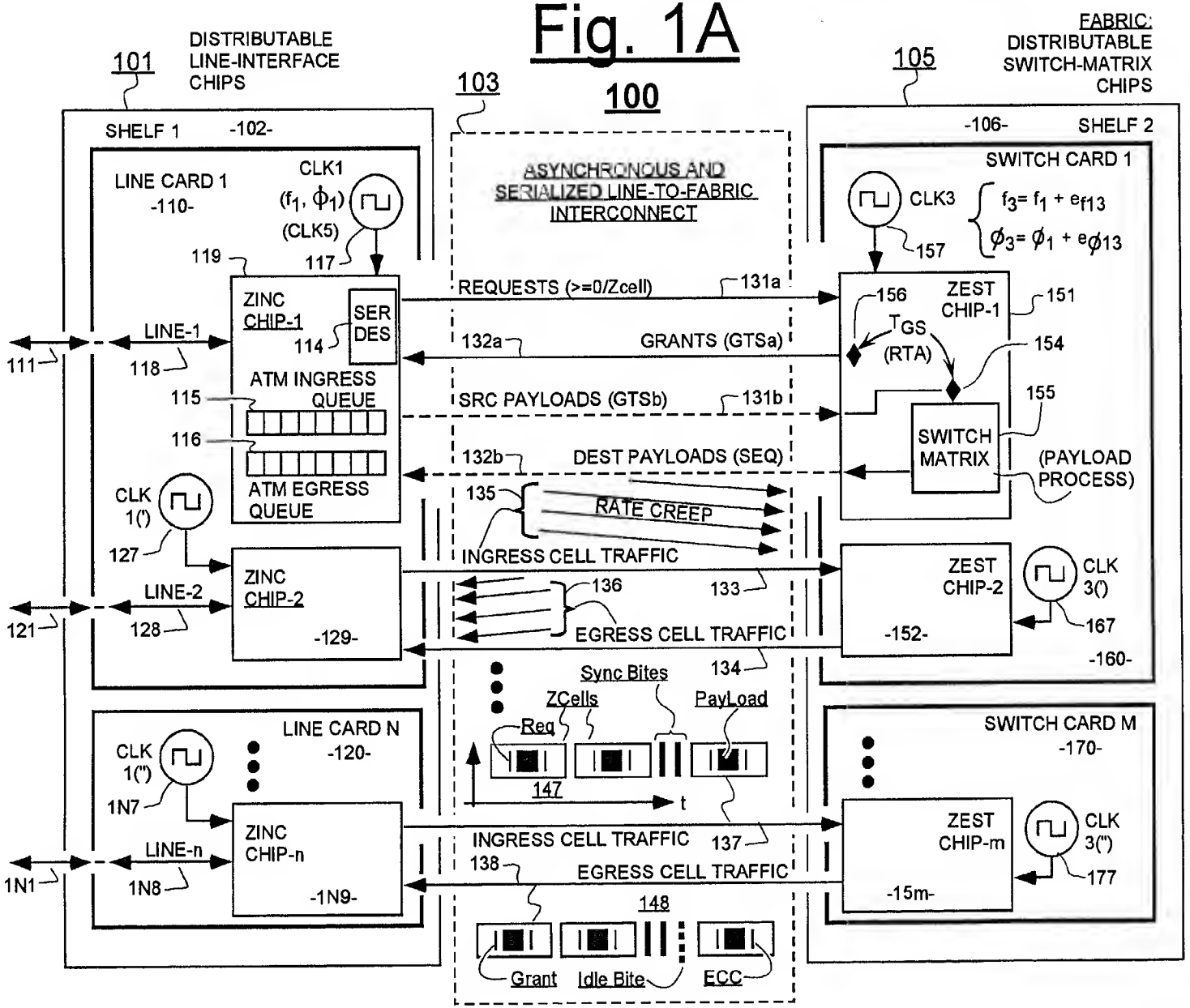
Fig. 1A



MAIN CONCEPTS

(1) CLOCK-TREE FREE SCALABILITY

(2) DISTRIBUTABLE LINE-INTERFACE CHIPS (ZINCS)

(3) DISTRIBUTABLE SWITCH-MATRIX CHIPS (ZESTS)

(4) WIRES SAVINGS DUE TO SERIAL--IZED & ASYNCH--RONOUS ZINC-ZEST LINKS

(5) FABRIC-USE ARBITRATION

(6) SWITCH-THRU SCHEDULING

(7) BUFFER-OVER-LOAD PREVEN--TION

(8) ERROR CORRECTION (SAFETY MARGIN FOR NON-REPEAT THROUGH-PUT)

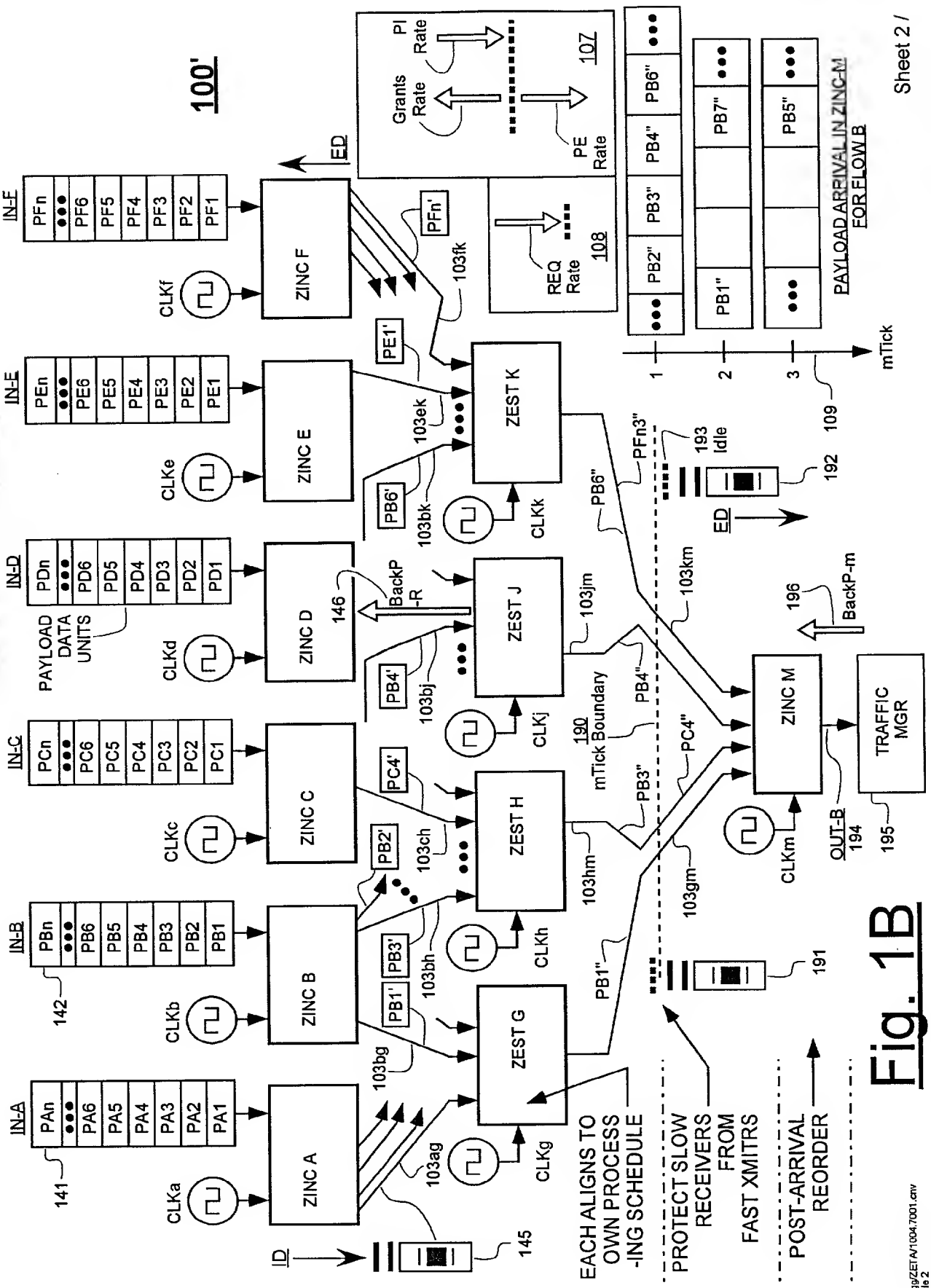


Fig. 1B

Sheet 2 /

ggg/ZETA/1004.7001.cnv
Tile 2
ver 4/09/2001 pm 1:30

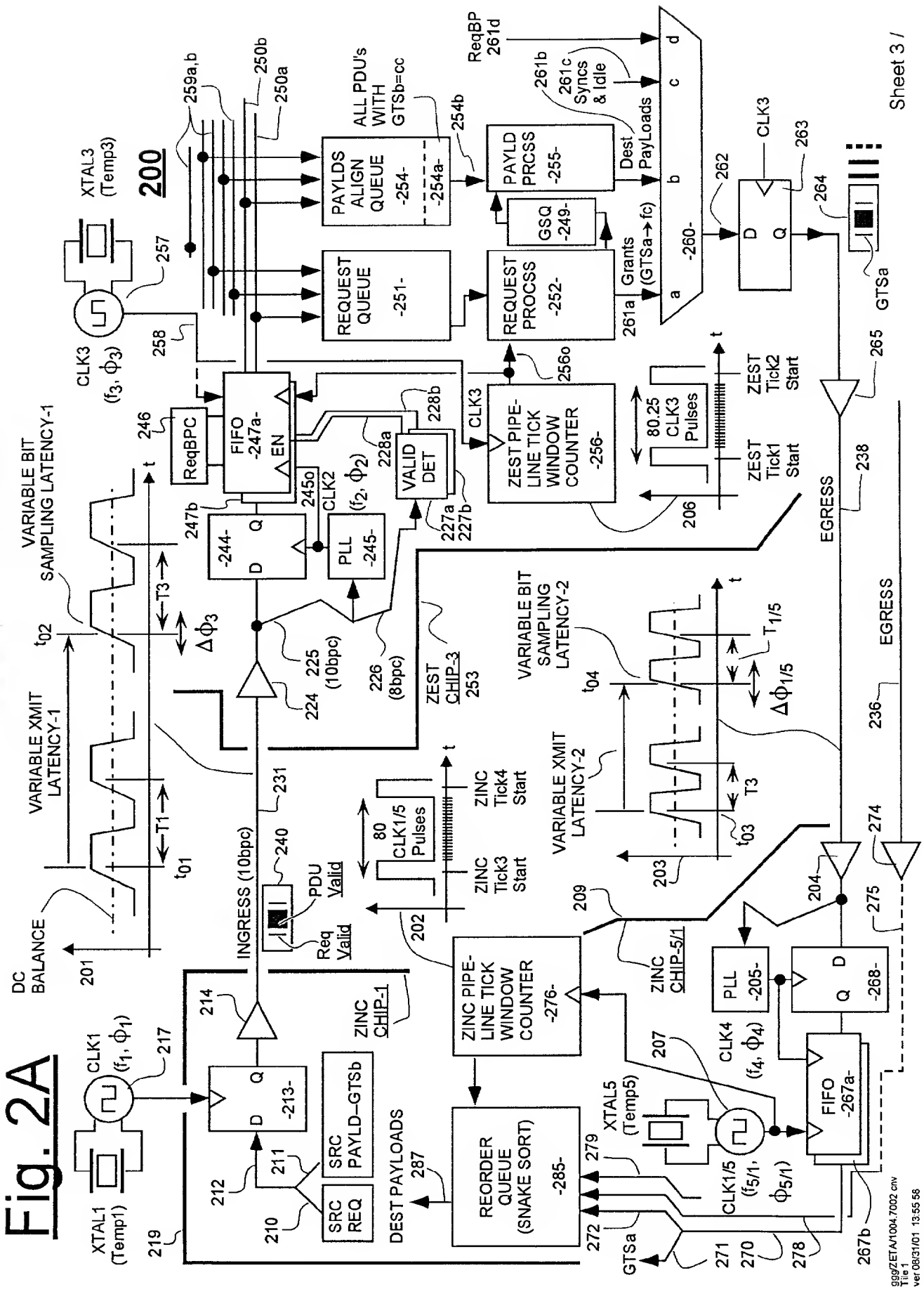
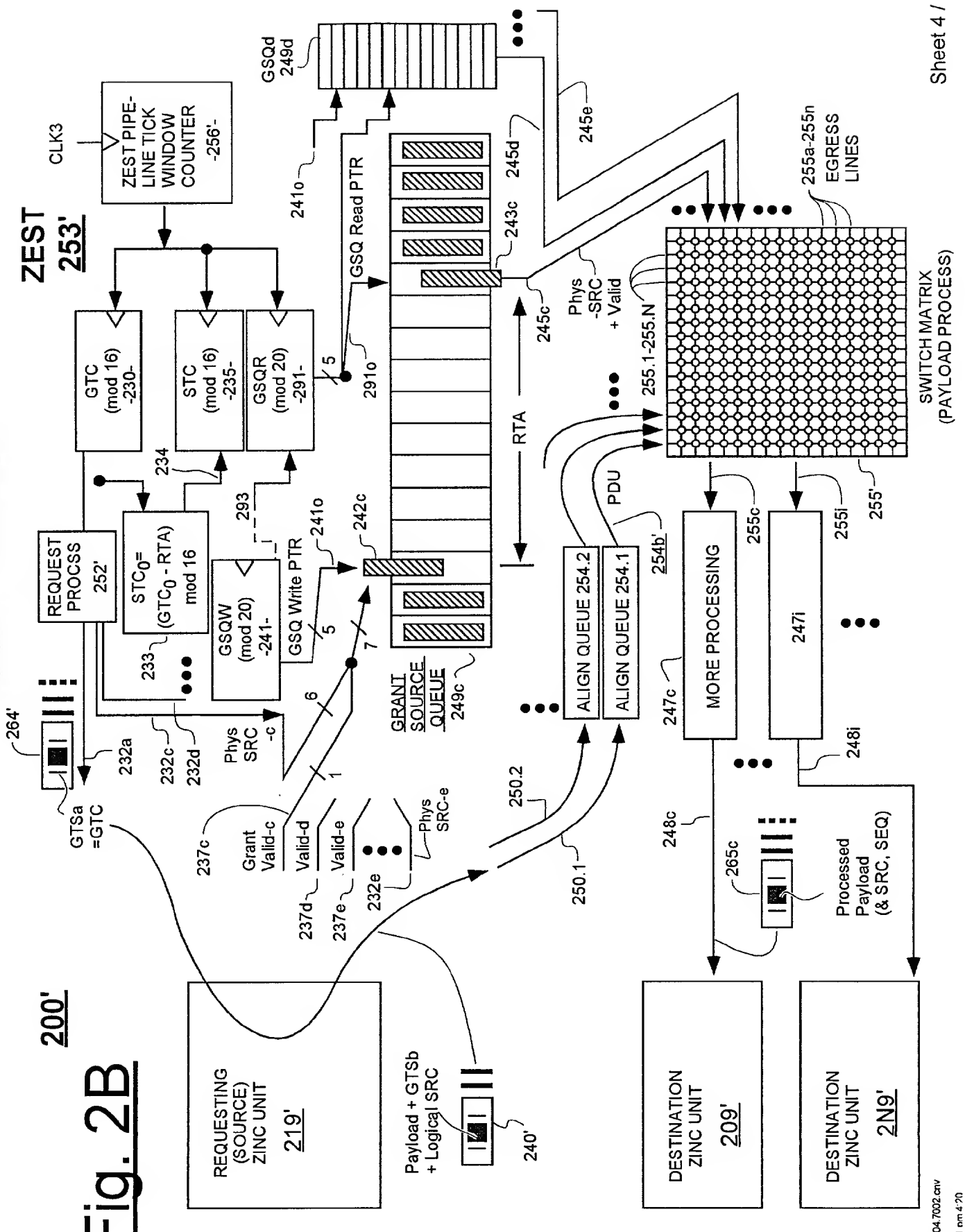

200
XTAL1 (Temp1)
CLK1 (f_1, ϕ_1)
XTAL3 (Temp3)
CLK3 (f_3, ϕ_3)
XTAL5 (Temp5)
CLK4 (f_4, ϕ_4)
CLK1/5 ($f_{5/1}$, $\phi_{5/1}$)
CLK2 (f_2, ϕ_2)
DC BALANCE
VARIABLE XMIT LATENCY-1
VARIABLE BIT SAMPLING LATENCY-1
VARIABLE XMIT LATENCY-2
VARIABLE BIT SAMPLING LATENCY-2
INGRESS (10bpc)
EGRESS
ZINC CHIP-1
ZEST CHIP-3
ZINC CHIP-5/1
SRC PAYLD–GTSb
SRC REQ
DEST PAYLOADS
REORDER QUEUE (SNAKE SORT) -285-
ZINC PIPE-LINE TICK WINDOW COUNTER -276-
ZEST PIPE-LINE TICK WINDOW COUNTER -256-
REQUEST QUEUE -251-
REQUEST PROCSS -252-
PAYLDS ALIGN QUEUE -254-
PAYLD PRCSS -255-
GSQ -249-
FIFO -247a- EN
FIFO -267a-
VALID DET
PLL -245-
PLL -205-
ReqBPC
ReqBP 261d
ALL PDU's WITH GTSb=cc
Dest PayLoads
Grants (GTSa→fc)
Syncs & Idle
GTSa
PDU Valid
Req Valid
80 CLK1/5 Pulses
80.25 CLK3 Pulses
ZINC Tick3 Start
ZINC Tick4 Start
ZEST Tick1 Start
ZEST Tick2 Start
Sheet 3 /
ggg/ZETA/1004.7002 cnv
Tile 1
ver 08/31/01 13:55 58

Fig. 2A


200'
ZEST 253'
CLK3
ZEST PIPE-LINE TICK WINDOW COUNTER -256'-
GSQd 249d
241o
GSQ Read PTR
291o
GTC (mod 16) -230-
STC (mod 16) -235-
GSQR (mod 20) -291-
REQUEST PROCESS 252'
STC0= (GTC0 - RTA) mod 16
GSQW (mod 20) -241-
GSQ Write PTR
GRANT SOURCE QUEUE 249c
242c
243c
245d
245e
245c
RTA
Phys -SRC + Valid
255.1-255.N
SWITCH MATRIX (PAYLOAD PROCESS)
255a-255n EGRESS LINES
PDU
254b'
ALIGN QUEUE 254.2
ALIGN QUEUE 254.1
MORE PROCESSING
247c
247i
255c
255i
255'
248i
248c
265c
Processed Payload (& SRC, SEQ)
250.1
250.2
GTSa =GTC
264'
232a
232c
232d
Phys SRC -c
233
234
293
237c
Grant Valid-c
Valid-d
Valid-e
Phys SRC-e
237d
237e
232e
REQUESTING (SOURCE) ZINC UNIT 219'
Payload + GTSb + Logical SRC
240'
DESTINATION ZINC UNIT 209'
DESTINATION ZINC UNIT 2N9'
Sheet 4 /
Fig. 2B
ggg/ZETA/1004.7002.cnv
Title 2
ver 5/22/2001 pm 4:20

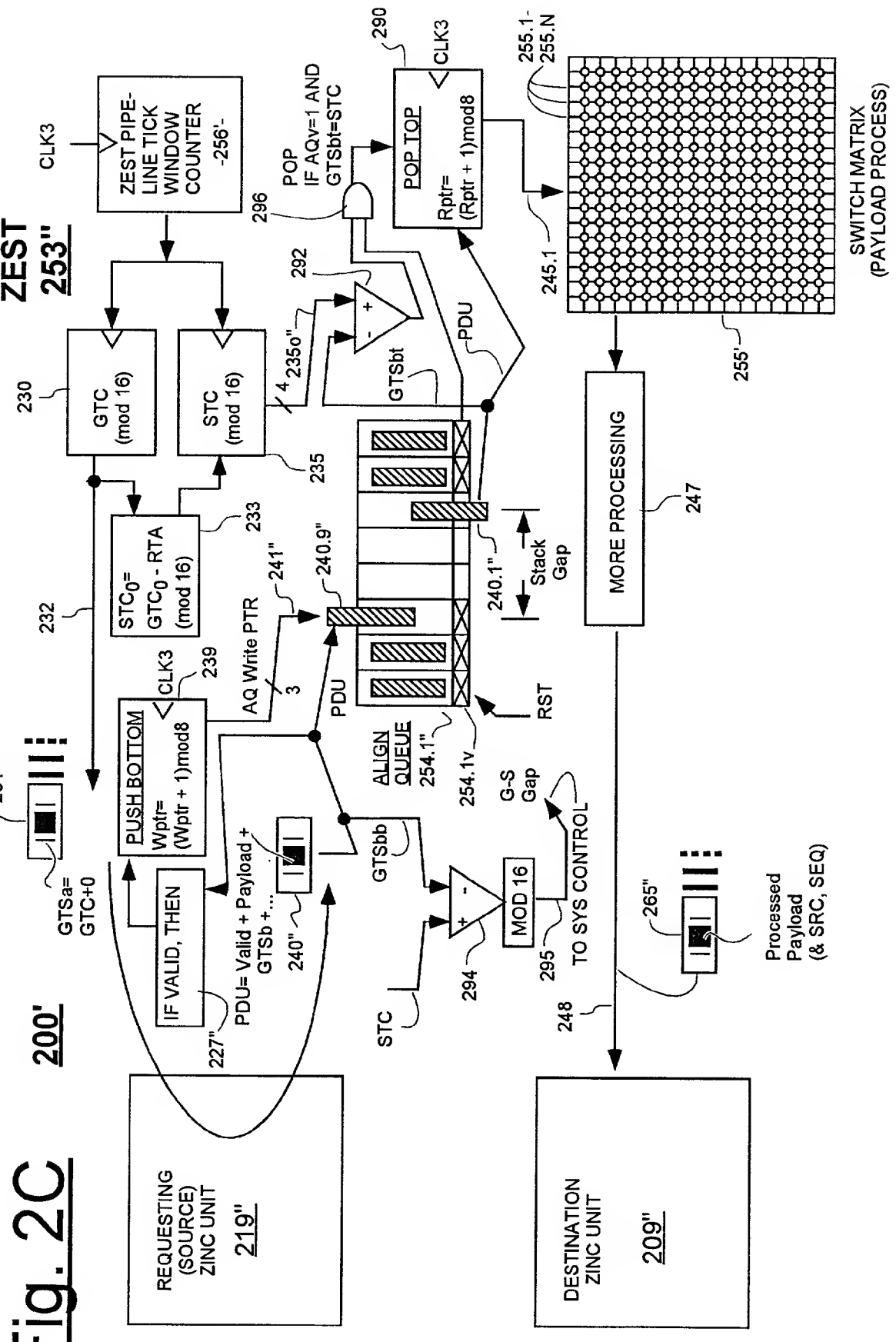


Fig. 2C

200'

Sheet 5 /

ggg/ZETA/1004.7002.cnv
Tile 3
ver 4/10/2001 pm 12:30

Fig. 3

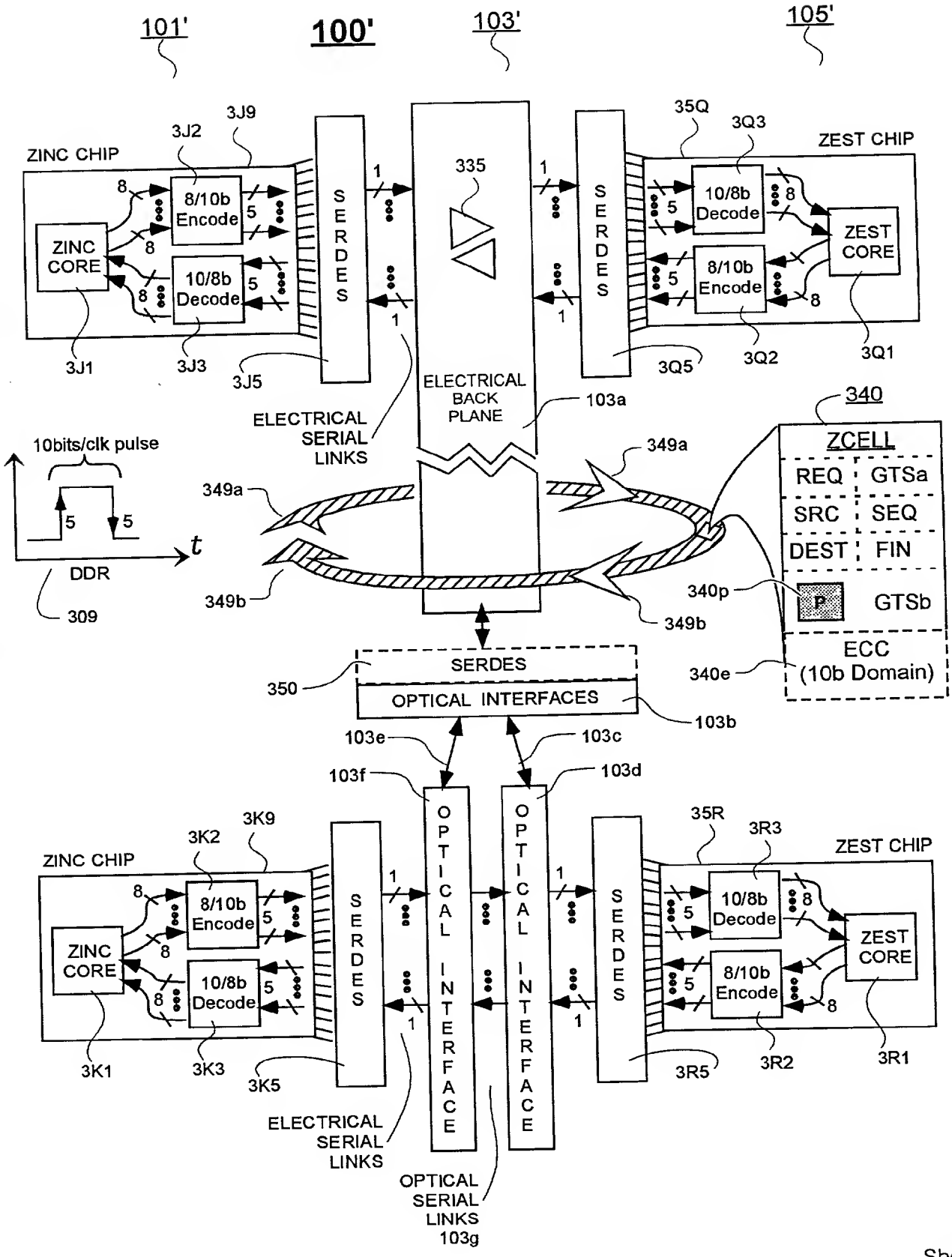

101'
100'
103'
105'
ZINC CHIP
ZINC CORE
8/10b Encode
10/8b Decode
SERDES
ELECTRICAL SERIAL LINKS
ELECTRICAL BACK PLANE
335
ZEST CHIP
ZEST CORE
10bits/clk pulse
DDR
309
340
ZCELL
REQ
GTSa
SRC
SEQ
DEST
FIN
P
GTSb
ECC (10b Domain)
SERDES
OPTICAL INTERFACES
OPTICAL INTERFACE
OPTICAL SERIAL LINKS 103g

Fig. 4

400

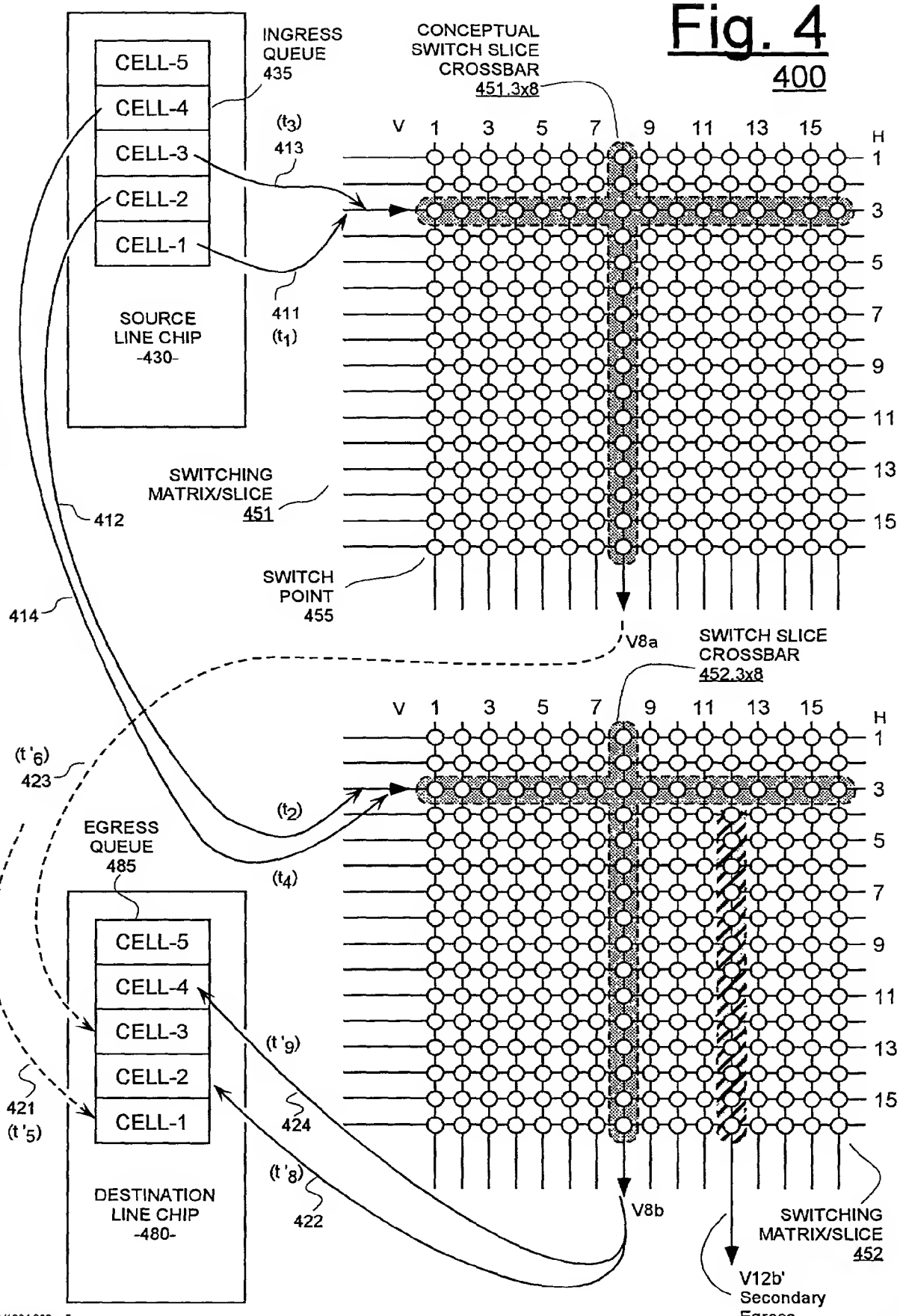
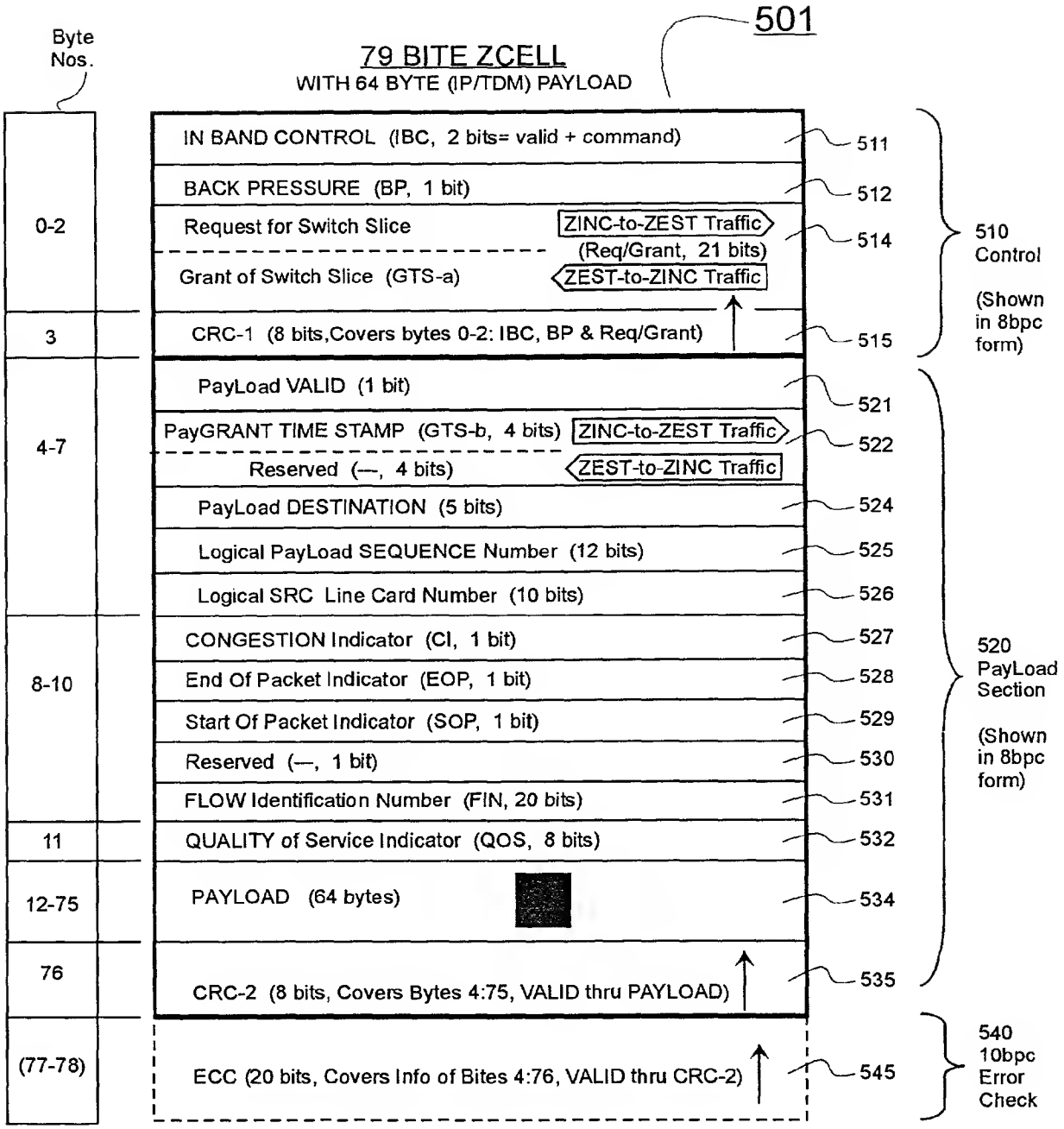

CELL-5
CELL-4
CELL-3
CELL-2
CELL-1
INGRESS QUEUE 435
SOURCE LINE CHIP -430-
CONCEPTUAL SWITCH SLICE CROSSBAR 451.3x8
V 1 3 5 7 9 11 13 15
H 1 3 5 7 9 11 13 15
(t3) 413
411 (t1)
SWITCHING MATRIX/SLICE 451
412
414
SWITCH POINT 455
V8a
SWITCH SLICE CROSSBAR 452.3x8
(t'6) 423
(t2)
(t4)
EGRESS QUEUE 485
(t'9)
424
421 (t'5)
(t'8)
422
DESTINATION LINE CHIP -480-
V8b
SWITCHING MATRIX/SLICE 452
V12b' Secondary Egress

Fig. 5A


501
79 BITE ZCELL
WITH 64 BYTE (IP/TDM) PAYLOAD
Byte Nos.
0-2
3
4-7
8-10
11
12-75
76
(77-78)
IN BAND CONTROL (IBC, 2 bits= valid + command)
BACK PRESSURE (BP, 1 bit)
Request for Switch Slice
ZINC-to-ZEST Traffic
(Req/Grant, 21 bits)
Grant of Switch Slice (GTS-a)
ZEST-to-ZINC Traffic
CRC-1 (8 bits,Covers bytes 0-2: IBC, BP & Req/Grant)
PayLoad VALID (1 bit)
PayGRANT TIME STAMP (GTS-b, 4 bits)
ZINC-to-ZEST Traffic
Reserved (—, 4 bits)
ZEST-to-ZINC Traffic
PayLoad DESTINATION (5 bits)
Logical PayLoad SEQUENCE Number (12 bits)
Logical SRC Line Card Number (10 bits)
CONGESTION Indicator (CI, 1 bit)
End Of Packet Indicator (EOP, 1 bit)
Start Of Packet Indicator (SOP, 1 bit)
Reserved (—, 1 bit)
FLOW Identification Number (FIN, 20 bits)
QUALITY of Service Indicator (QOS, 8 bits)
PAYLOAD (64 bytes)
CRC-2 (8 bits, Covers Bytes 4:75, VALID thru PAYLOAD)
ECC (20 bits, Covers Info of Bites 4:76, VALID thru CRC-2)
511
512
514
515
521
522
524
525
526
527
528
529
530
531
532
534
535
545
510 Control (Shown in 8bpc form)
520 PayLoad Section (Shown in 8bpc form)
540 10bpc Error Check

ZINC-to-ZEST Traffic

21-bit UNICAST REQUEST FIELD

Fig. 5B

514B

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M = 0	V 1	Primary Priority Code			Primary Egress Line						V 2	Secondary Priority Code			Secondary Egress Line					
550	551	552			553						555	556			557					

ZINC-to-ZEST Traffic

21-bit MULTICAST REQUEST FIELD

Fig. 5C

514C

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M = 1	V 1	Multicast Request Priority			Multicast Request Label												Reserved			
560	561	562			563												564			

ZEST-to-ZINC Traffic

21-bit NonTDM Unicast GRANT FIELD

514D

Fig. 5D

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M = 0	V 1	0	Reserved		Expansion						VOQ #						GTS-a			
					Grant Label															
570	571	572	573		574												575			

ZEST-to-ZINC Traffic

21-bit NonTDM Multicast GRANT FIELD

514E

Fig. 5E

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M = 1	V 1	0	Reserved		Multicast Grant Label (Grant LookUp Table Address)												GTS-a			
580	581	582	583		584												585			

ZEST-to-ZINC Traffic

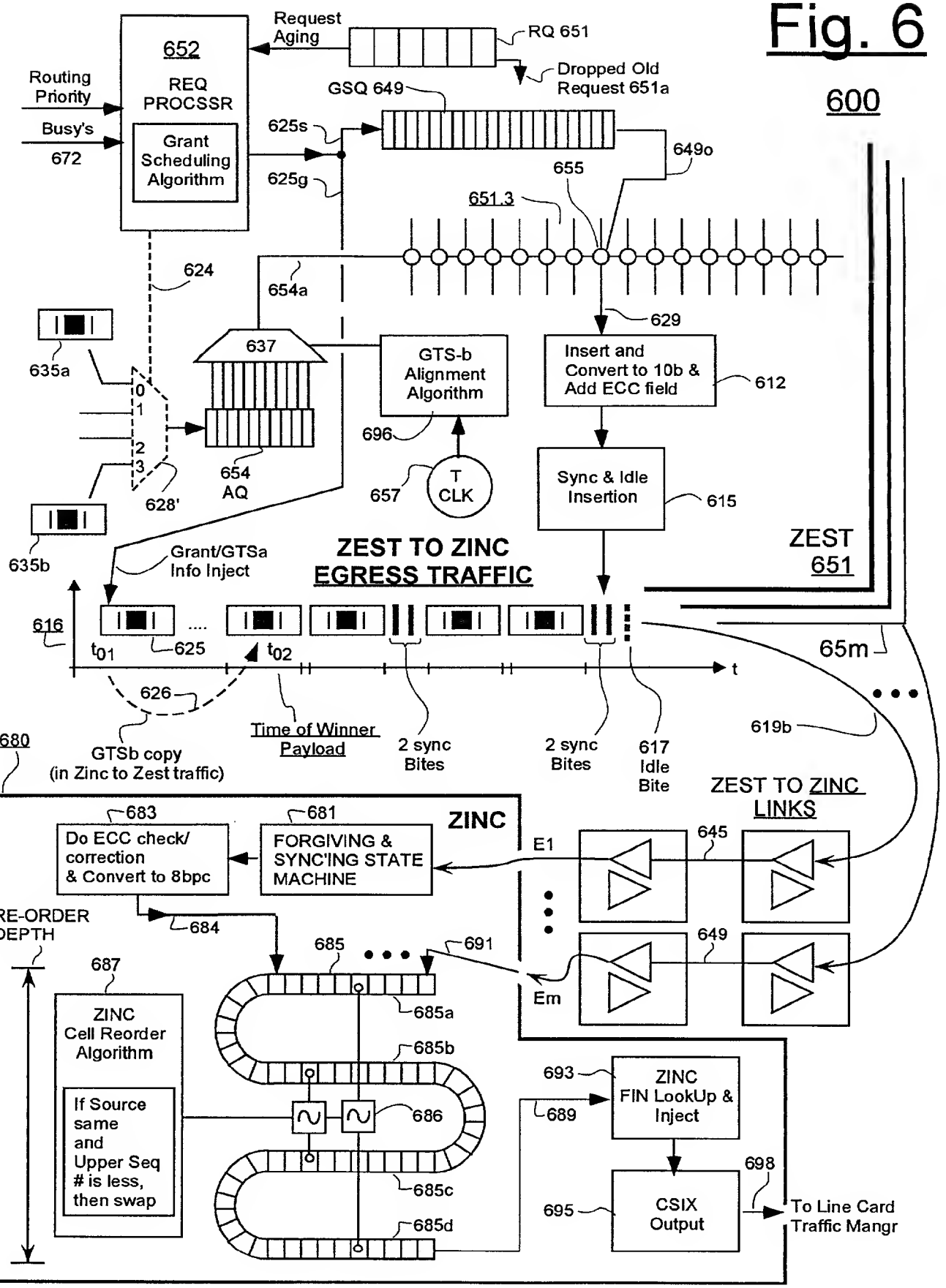
21-bit TDM GRANT FIELD

514F

Fig. 5F

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M	V 1	T = 1	Reserved		ZEST Slot Number				TDM Channel Number								GTS-a			
590	591	592	593		594				596								595			

Fig. 6


600
652
REQ PROCSSR
Grant Scheduling Algorithm
Routing Priority
Busy's
672
Request Aging
RQ 651
Dropped Old Request 651a
GSQ 649
625s
625g
649o
655
651.3
624
654a
629
635a
637
GTS-b Alignment Algorithm
Insert and Convert to 10b & Add ECC field
612
696
654 AQ
628'
657
T CLK
Sync & Idle Insertion
615
635b
Grant/GTSa Info Inject
ZEST TO ZINC EGRESS TRAFFIC
ZEST 651
616
625
t_{01}
t_{02}
t
626
65m
619b
680
GTSb copy (in Zinc to Zest traffic)
Time of Winner Payload
2 sync Bites
2 sync Bites
617 Idle Bite
ZEST TO ZINC LINKS
ZINC
683
Do ECC check/ correction & Convert to 8bpc
681
FORGIVING & SYNC'ING STATE MACHINE
E1
645
649
Em
691
RE-ORDER DEPTH
684
685
687
ZINC Cell Reorder Algorithm
If Source same and Upper Seq # is less, then swap
685a
685b
686
685c
685d
693
ZINC FIN LookUp & Inject
689
698
695
CSIX Output
To Line Card Traffic Mangr

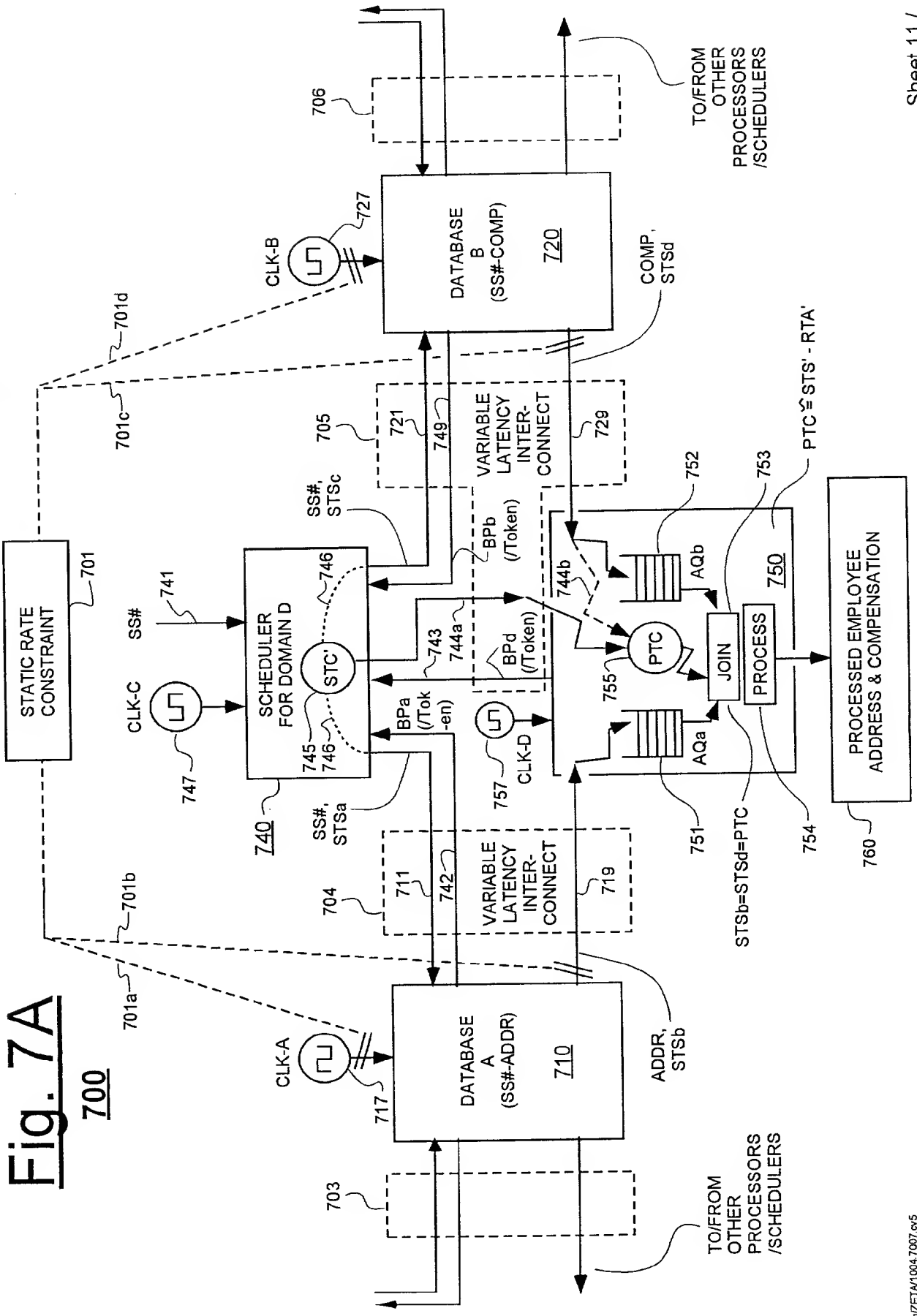


Fig. 7A

Sheet 11 /

999/ZETA/1004.7007.cv5
Tile 1
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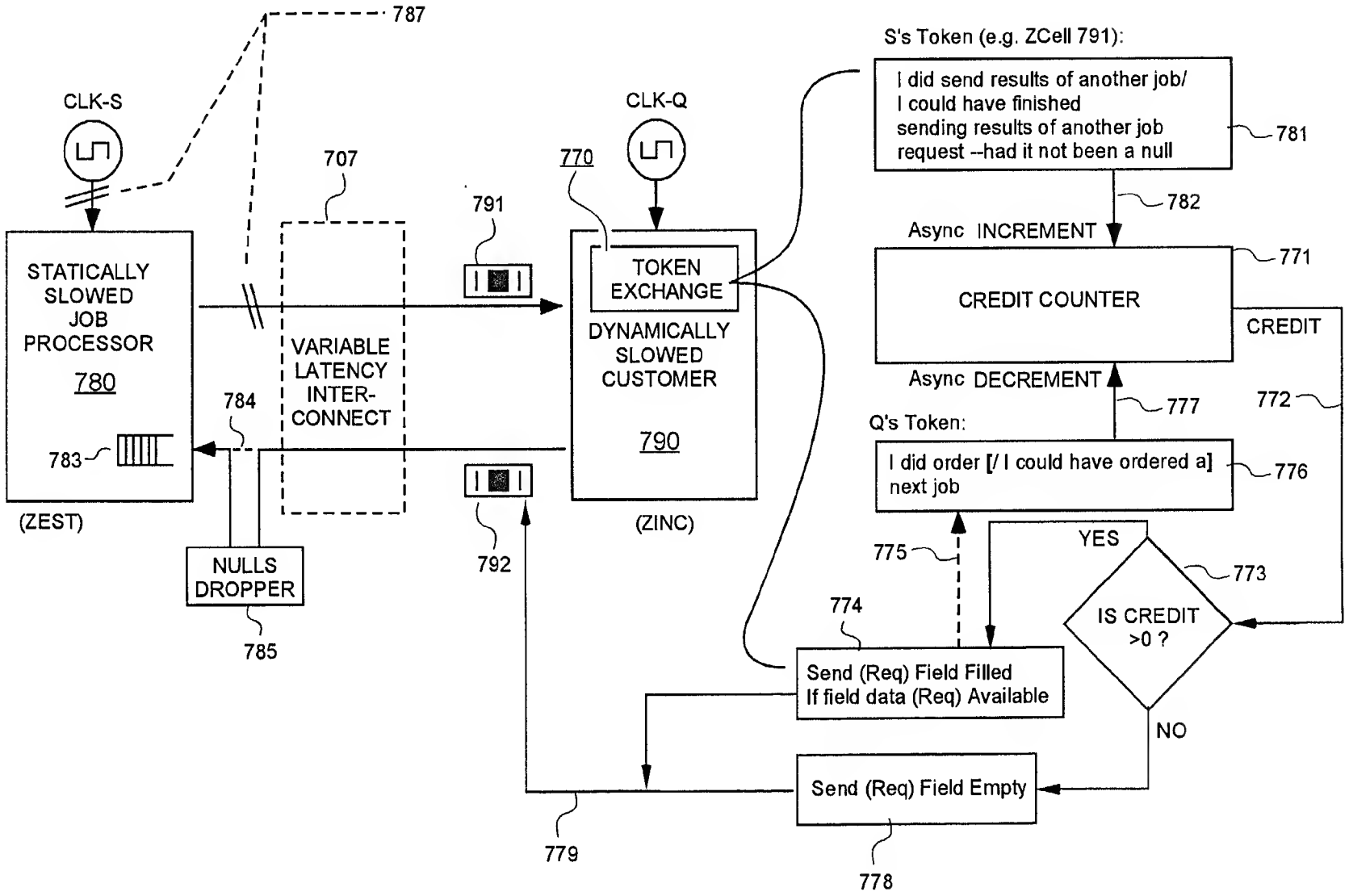
Fig. 7B


787
CLK-S
CLK-Q
707
770
791
S's Token (e.g. ZCell 791):
I did send results of another job/
I could have finished
sending results of another job
request --had it not been a null
781
782
Async INCREMENT
771
CREDIT COUNTER
CREDIT
772
Async DECREMENT
777
Q's Token:
I did order [/ I could have ordered a]
next job
776
STATICALLY
SLOWED
JOB
PROCESSOR
780
783
784
VARIABLE
LATENCY
INTER-
CONNECT
TOKEN
EXCHANGE
DYNAMICALLY
SLOWED
CUSTOMER
790
(ZEST)
(ZINC)
NULLS
DROPPER
785
792
775
YES
773
IS CREDIT
>0 ?
774
Send (Req) Field Filled
If field data (Req) Available
NO
Send (Req) Field Empty
779
778